UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,513	08/17/2001	Yves Morand	00-CCL-096	6322

23334 7590 05/14/2003

FLEIT, KAIN, GIBBONS,
GUTMAN & BONGINI, P.L.
ONE BOCA COMMERCE CENTER
551 NORTHWEST 77TH STREET, SUITE 111
BOCA RATON, FL 33487

EXAMINER
LEE, HSIEN MING

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,513	MORAND ET AL.	
	Examiner	Art Unit	
	Hsien-Ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-13 and 15-18* is/are rejected.

7)☒ Claim(s) *8,14 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4)☐ Interview Summary (PTO-413) Paper No(s). _____
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other.

DETAILED ACTION

Remarks

1. The 112-second-paragraph rejection to claim 8 and the 102(e) rejection to claims 1-18 are withdrawn in response to applicant's amendment filed 2/27/03.

Claim Objections

2. Claims 8, 14 and 16 are objected to because of the following informalities: the inconsistent terminology, i.e. "trench" versus "conducting trench." Changing the "trench" (i.e. as recited in claim 8, line 3, claim 14, line 1 and claim 16, line 1) into " **conducting** trench" is suggested.

Claim 14, at line 2, "comprises only the conducting material forming the lower electrode" should be -- comprises only **a** conducting material forming the lower electrode --. Claim 16, at lines2-3, "by the conducting material forming the lower electrode" should be -- by **a** conducting material forming the lower electrode --. (Emphasis added) Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-7, 9-13 and 15-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitations recited in the amended claims renders indefinite due to ambiguous descriptions. Based on the best comprehension of the Examiner (refers to Fig.5 and related text), the claim body of claim 1 may be rewritten as follows:

- producing several metallization levels (i.e. M1 and M2), which are mutually separated by **an** interlevel insulating **layer** (i.e.2);
- producing intertrack insulating layers (i.e. 3 and 8), each separating tracks (80 and 81) of the same metallization level (i.e. M2);
- producing at least one capacitor comprising a lower electrode (i.e. 50) and an upper electrode (i.e. 70) which are mutually separated by a dielectric layer (i.e. 60); wherein the producing the at least one capacitor comprises:

  simultaneously producing, in at least part of an interlock insulating layer (i.e. 3) associated with **one of the several metallization levels**, the lower electrode, the upper electrode, and the dielectric layer of the at least one capacitor;

  simultaneously producing a conducting trench (i.e. 41) which laterally extends the lower electrode (i.e. 50) of the **at least one capacitor and is** electrically isolated from the upper electrode (i.e. 70) and has a traverse dimension smaller than the traverse dimension of the **at least one** capacitor; and

- producing, **in the intertrack insulating layers** (i.e. 3 and 8), two conducting pads (i.e. 80 and 81) which come into contact with the upper electrode (i.e. 70) of the **at least one** capacitor and with the conducting trench (i.e. 41), respectively.

In re amended claim 2, it may be rewritten as follow:

The process according to Claim 1, wherein the **conducting** trench comprises only **a** conducting material forming the lower electrode.

In re amended claims 3, 13, 15 and 17, they may be written as follow:

The process according to Claim 1, wherein the tracks **of the one of the several** metallization level are produced simultaneously with **the producing of the upper electrode of the at least one capacitor.**

In re amended claim 4, it may be written as follow:

The process according to Claim 1, wherein the **producing** of the **at least** capacitor and of the **conducting** trench comprises:

a) **forming one of** the intertrack insulating layers (i.e. 3) on **the** interlevel insulating layer (i.e. 2); b) etching at least part of **the one of** the intertrack insulating layers **to** form a cavity having a main part laterally extended by the **conducting** trench; c) **forming** a first conducting layer of a first conducting material **in the cavity and the conducting trench** obtained in step b) and **forming** a dielectric layer of a dielectric material on the first conducting layer; d) **forming** a second conducting layer of a second conducting material on the dielectric layer **to** fill the main part of the cavity, **wherein** the dimensions of the **conducting** trench and the thickness of the first conducting layer and of the dielectric layer being chosen **to** obtain, after step d), **the conducting** trench comprising at least the first conducting material but not containing the second conducting material; and e) chemical-mechanical polishing **the first conducting layer, the dielectric layer and the second conducting layer to form the at least one capacitor** in the main part of the

cavity, **wherein** the lower electrode is formed from a residual part of the first **conducting** layer **resided** in internal walls of the cavity and **the** upper electrode is formed from a residual part of the second **conducting** layer, which is separated from the residual part of the first **conducting** layer by a residual part of the dielectric layer; **and** to **leave another** residual part of the first **conducting layer in the conducting trench**.

In re amended claims 5 and 9, they may be written as follow:

The process according to Claim 4, wherein the **conducting** trench comprises only the **first** conducting **layer** forming the lower electrode.

In re claims 6 and 10, they may be written as follow:

The process according to Claim 4, wherein the tracks of **one of the several metallization levels** are produced simultaneously with the **producing** of the upper electrode of the **at least** capacitor.

In re claims 7 and 11, they may be written as follow:

The process according to Claim 4, wherein the producing of the tracks of **one of the several metallization level**s comprises:

after step c), etching the dielectric layer of the first conducting layer and of the intertrack insulating layer **to** form at least one auxiliary trench; the formation of the second conducting layer being carried out in step d) **to** substantially fill the **conducting** trench; and **chemical-**

mechanical polishing to remove the first conducting layer, the dielectric layer and the second conducting layer from the surface of the intertrack insulating layer.

In re claims 12, it may be written as the following format:

An integrated circuit, comprises:

- several metallization levels which are mutually separated by interlevel insulating layers;
- intertrack insulating layers, each of the interlock insulating layers separating the tracks of the same metallization level;
- at least one capacitor comprising a lower electrode and an upper electrode which are mutually separated by a dielectric layer, wherein the **at least one** capacitor is located in at least part of an intertrack insulating layer associated with **one of the several** metallization levels; the lower electrode of the **at least one** capacitor is laterally extended by a conducting trench, which is electrically isolated from the upper electrode and has a transverse dimension smaller than the transverse dimension of the capacitor; and **one of** the interlevel insulating **layers** covering the intertrack insulating layer; and
- two conducting pads which come into contact with the upper electrode of the **at least** capacitor and with the conducting trench, respectively.

In re claims 18, it may be written as the following format:

An integrated circuit comprising:

- a plurality of metallization levels that are mutually separated by interlevel insulating layers,
- **a plurality of** intertrack insulating layers, each of the intertrack insulating layers separating the tracks of the same metallization level; and
- at least one capacitor comprising a lower electrode and an upper electrode, which are mutually separated by a dielectric layer, and wherein the capacitor is located in at least part of an intertrack insulating layer associated with **one of the plurality of** metallization level**; and** the lower electrode of the **at least one** capacitor is laterally extended by a conducting trench, which is electrically isolated from the upper electrode and has a transverse dimension smaller than the transverse dimension of the capacitor, and the interlevel insulating layer covering the intertrack insulating layer; and
- two conducting pads come into contact with the upper electrode of the **at least one** capacitor and with the conducting trench, respectively, and wherein the tracks of **one of the plurality of metallization levels** are formed from the **same** material as that **of** the upper electrode of the **at least one** capacitor.

In addition, the limitation " the trench comprises only the **dielectric encapsulated by the conducting material** forming the lower electrode" as recited in claim **16** is unclear to the Examiner because the conducting trench only contains a conducting material, **not** including any dielectric material, as illustrated in Figs. 5 and 11. (Emphasis added)

Allowable Subject Matter

5. Claims 8 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 1,12 and 18 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

7. Claims 2-7, 9-11, 13 and 15-17 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record, Brabazon et al. to US 6,008,083, teaches a method for fabricating an integrated circuit (Figs. 10-13), the method comprising the steps of:

- producing several metallization levels (i.e. first level 10, second level 54/56 and third level 74/76/78), which are mutually separated by an interlevel insulating layer 52;
- producing intertrack insulating layers 72, each separating tracks 74, 76 and 78 of the same metallization level;
- producing at least one capacitor comprising a lower electrode 62 and an upper electrode 68 which are mutually separated by a dielectric layer 66; wherein the producing the at least one capacitor comprises:

  simultaneously producing, in at least part of an interlock insulating layer 58 associated with a particular metallization level 62/68 and 64, the lower electrode 62, the upper electrode 68, and the dielectric layer 66 of the at least one capacitor;

simultaneously producing a conducting trench 64 electrically isolated from the upper electrode 68 and has a traverse dimension smaller than the traverse dimension of the capacitor; and

- producing, in the intertrack insulating layers 72, two conducting pads 76 and 78

which come into contact with the upper electrode 68 of the capacitor and with the conducting trench 64, respectively.

In contrast, Brabazon et al neither teach nor suggest simultaneously producing the conducting trench which *laterally extends the lower electrode* of the at least one capacitor.

Bernstein et al. to US 6,452,251 teach a method for fabricating an integrated circuit (Fig.1K), the method comprising the steps of :

- producing several metallization levels (i.e. first level 23/25, second level 41C/43B, 41/43C and third level 75/77, which are mutually separated by an interlevel insulating layer 27/29;
- producing intertrack insulating layers 73, each separating tracks 75 and 77 of the same metallization level;
- producing at least one capacitor comprising a lower electrode 41B and an upper electrode 55 which are mutually separated by a dielectric layer 49A; wherein the producing the at least one capacitor comprises:

simultaneously producing, in at least part of an interlock insulating layer 29 associated with a particular metallization level 41B/51A and 41C/43B and 41, the lower electrode 41B, the upper electrode 55, and the dielectric layer 49A of the at least one capacitor;

simultaneously producing a conducting trench 41 electrically isolated from the upper electrode 55; and

- producing, in the intertrack insulating layers 73, two conducting pads 75 and 77 which come into contact with the upper electrode 55 of the capacitor and with the conducting trench 41, respectively.

In contrast, Bernstein et al neither teach nor suggest simultaneously producing the conducting trench 41 which *laterally extends the lower electrode* 41B of the at least one capacitor because the conducting trench 41 is electrically isolated to the lower electrode 41B of the capacitor by an insulating layer 71 (Fig.1K). Bernstein et al also neither teach nor suggest that conducting trench 41 has a traverse dimension *smaller than* the traverse dimension of the capacitor.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

W David Coleman
Primary Examiner
Art Unit 2823

Hsien Ming Lee
May 6, 2003